

3-D Architectures for Semiconductor Integration and Packaging

The Practical and Competitive Landscape on the Path to Implementation

December 9–11, 2009

Hyatt Regency San Francisco Airport Hotel, Burlingame, California

3-D integration and packaging represents a paradigm shift for the semiconductor industry. This shift opens up entirely new pathways for performance advancement, and offers new prospects for industry growth. The equipment market alone is anticipated to exceed \$1 billion within the next few years. No doubt there are many challenges remaining though, before widescale implementation occurs. Those industry players, however, who understand these challenges, and offer new solutions, will reap the rewards over the coming decades.

The first conference in this series took place in 2004, long before 3-D integration and through-silicon-vias (TSV) became the buzzwords they are today. Since then, this conference series has continued to provide a unique perspective of this emerging commercial opportunity, combining technology with business: research developments with practical insights, to offer industry leaders the information needed to plan and move forward with confidence.

This conference, **3-D Architectures for Semiconductor Integration and Packaging**, targets senior-level technologists, managers, and executives from leading companies and organizations from around the world, and addresses the interests of a diverse group:

End Users	Electronic systems producers
Device designers	Materials and equipment suppliers
Semiconductor fabs	EDA suppliers
Integrated device manufacturers	Research institutions
Fabless semiconductor cos.	Government agencies
Packaging houses	Investment and business development advisors

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<http://techventure.rti.org>

Also attend...

**The Latest Views and Analysis on
3-D Integration, TSV
Processing, and Reliability**

Details inside

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Preconference Symposium The Latest Views and Analysis on 3-D Integration, TSV Processing, and Reliability

9 December 2009

12:30 pm – 5:30 pm

Attend this pre-conference symposium to gain important new insights on 3-D integration technology, manufacturing, and implementation issues – including important new perspectives on TSV processing and reliability. Join these industry leaders for a half-day of an intensive look at some of the key elements of today's race toward the development and implementation of 3-D technology.

3-D Integration Technology and Industry Update

Philip Garrou, *IEEE Fellow and Consultant*

Microelectronic Consultants of NC

- The range of process options are narrowing
- Reliability issues and concerns -- p-Si vs. Cu vs. W
- Factors to consider in looking at various bonding technologies
- What is happening around the world at the leading and emerging 3-D R&D Institutes and Consortia

Thermo-Mechanical Reliability Challenges of 3-D Integration

Paul Ho, *Professor and Director of the Laboratory for*

Interconnect and Packaging, University of Texas at Austin

- Problem synopsis
- Process-induced stresses for TSV structures
- Impact on interfacial fracture and device performance
- Power dissipation and electromigration

TSV Technology Implementation – Design, Process, and Reliability Studies for Product Applications

Nagesh Vodrahalli, *VP Technology and Manufacturing, ALLVIA*

- TSV technology overview
- Critical factors and challenges in TSV design, process, and reliability
- Implementation of TSV technology – test vehicles, reliability results, and product examples
- Future outlook – critical needs, challenges, and the prognosis

Production Processing of High Aspect-Ratio TSVs

Claudio Truzzi, *CTO, Alchimer*

- TSV processing represents key challenge to industry-wide adoption of 3-D IC solutions
- Review of current TSV metallization – iPVD and CVD/ALD – performance and costs
- A novel electrografting approach – process and cost considerations
- Film property and reliability data
- Third-party cost-of-ownership analysis

Whether looking to come up the learning ramp, or a seasoned industry leader looking to get new perspectives around the latest insights, this pre-conference symposium is a key benefit of this conference experience.

9 December

1:00 pm – 5:30 pm Preconference Symposium

6:00 pm – 8:00 pm Registration and Welcome Reception

Sponsored By *Suss Microtech*

10 December

6:45 am – 8:00 am Registration and Continental Breakfast

8:00 am Welcome and Opening Comments

Conference Cochairs:

Robert Lanzone, *VP Advanced Packaging Development,*

Amkor Technology

Philip Garrou, *IEEE Fellow and Consultant,*

Microelectronic Consultants of NC

Keynote Session

The IDM and Foundry Perspective on 3-D Technology Trends and Opportunities

Interconnect Challenges for Next Generation Computing

Jerry Bautista, *Director of Technology Management,*

Microprocessor Research Laboratory, Intel

- Introduction/Problem Statement
- Why interconnect requirements are rising rapidly
- Potential solutions and tradeoffs
- Architectural implications

TSV Technology Challenges – From Wafer Foundry's Perspective

Douglas Yu, *Senior Director of Integrated Interconnect and*

Packaging Division of Corporate R&D,

Taiwan Semiconductor Manufacturing Company

Advancements in 3-D Technology for System Applications

John Knickerbocker, *Distinguished Engineer Manager:*

System on Package and 3-D Integration, IBM

- System trends
- Technology trends
- Advancements in 3-D technology
- 3-D system integration

10:00 am – 10:30 am Break

Looking Over the Horizon – Forecasting Growth

3-D Applications: 2009 is the Year of Full Volume Production

Jean-Christophe Eloy, *President and CEO, Yole Développement*

- Update of 3-D applications and roadmap
- Who is doing what and what products will be in production soon
- Updated market data and forecasts

3-D TSV Markets: Infrastructure Requirements for Growth

Jan Vardaman, *President, TechSearch International*

- Key 3-D TSV adoption applications
- Today's production volumes
- Potential markets for adoption
- Infrastructure issues and barriers for each application

On the Front – Applications Driving 3-D Development and Commercialization

3-D Finds the Road

Robert Patti, *CTO/VP, Tezzaron Semiconductor*

- Driving the market
- MPW work
- 3-D processing observations
- Evolving test
- 3-D commercialization

12:00 pm – 1:15 pm Lunch

Innovation through 3-D Integration: Opportunities and Challenges for a Wireless IC Company

Yann Guillou, *New Technology Marketing, 3-D Integration,*

ST-Ericsson

- Trends in mobile phones
- 3-D Integration: New opportunities and solutions to solve rising issues
- 3-D IC and TSV: A true paradigm shift
- 3-D Landscape: A new ecosystem required
- 3-D Application roadmap

Advanced Packaging and Integrated Passive Technologies to Improve Miniaturization and Reliability of Nomadic Devices

Franck Murray, *CEO, Ipdia*

- Integrated passives into silicon with a special focus on very high value 3-D capacitors
- Thin devices and miniaturization
- TSVs and 3-D packaging
- Application examples
- Improvement of reliability of integrated microsystems

Taking Advantage of 3-D - Rethinking Design Approaches

The Rochester Cube and Other 3-D Circuits for Clock and Power Delivery

Eby Friedman, *Professor, University of Rochester*

- 3-D power delivery and clock distribution
- TSV modeling
- The Rochester Cube
- Future 3-D design challenges
- Networks-on-chip
- Optimal via placement

3-D IC – An Advanced Packaging or a Silicon Technology?

Paul Franzon, *Alumni Distinguished Professor of Electrical and Computer Engineering, North Carolina State University*

- To truly exploit 3-D IC requires architectures specific for 3-D IC
- 3-D IC benefits from some modification in the CAD flow
- Partitioning is determined by CAD, DFT, and other practical issues
- Open issues

3:15 pm – 3:45 pm Break

Taller vs. Smaller: 3-D and Moore's Law

Frank Schellenberg, *Strategic Technology – Calibre RET*

Software, Design to Silicon Division, Mentor Graphics Corporation

- Traditional scaling and RET extensions to lithography
- 3-D and its impact on scaling
- Lessons learned from RET scaling
- Modeling insertion for 3-D: Design – Extraction – Interconnect – Test
- Design integration for 3-D

CAD Tools and Design Flow for 3-D Integration

Lisa McIlrath, *President/CEO, R²Logic*

- EDA requirements for the 3-D roadmap
- 3-D EDA must-haves
- Where adhoc fails
- 3-D EDA tool examples

3-D Thermal Analysis Application on a Two Stack Chip TSS

Vassilios Gerousis, *Sr. Product Marketing Manager/Sr. R&D*

Architect, Cadence Design Systems

- 3-D thermal analysis of two-chip TSS (Through Silicon TSV Stack)
- Can low power chips in vertical stack create hot spots?
- Modified design to be compatible with TSS
- 3-D IC thermal analysis and package thermal tool to construct boundary conditions
- Showing the impact of stacking on thermal maps of each chip

6:00 pm–8:00 pm Evening Reception

Sponsored By *EV Group*

11 December

6:45 am – 8:00 am Registration and

Continental Breakfast

Keynote Session

The Packaging Foundry and its Vital Role in Driving 3-D

3D ICs: The Next Revolution

Ho-Ming Tong, *Chief R&D Officer and General Manger of*

Group R&D, ASE Group

3-D Integration from an OSAT Perspective: The Past, the Present, and the Future

Raj Pendse, *VP Technology Group, STATS ChipPAC*

- Driver for 3-D integration
- The integration continuum: package-level, die-level, and everything in between
- Technology challenges and synergies
- Process partitioning and material flow logistics

3-D Packaging – View from the SAT

Ron Huemoeller, *VP, Advanced Interconnect,*

Amkor Technology

- Supply chain options
- Post TSV wafer processing wafer thinning—wafer thinning and processing
- 3-D Assembly: die-to-die vs. die-to-substrate—bonding and alignment

9:45 am – 10:15 am Break

Hotel Information

The Hyatt Regency San Francisco Airport Hotel is located 2 miles from the San Francisco International Airport and 14 miles south of San Francisco. Make your reservations by November 20 and mention you are attending RTI's 3-D Semiconductor conference to receive the \$169 room rate.

Hyatt Regency San Francisco Airport Hotel

1333 Bayshore Highway

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Fundamental Technology Approaches to Building 3-D

Direct Bond Interconnect (DBI®) – A Multi-dimensional Technology for Multi-dimensional ICs.

Paul Enquist, *CTO/Vice President R&D, Ziptronix*

- What is Direct Bond Interconnect?
- Different types of DBI®
- DBI® performance
- Adoption driving applications

Building Blocks Enabling Wafer Level Stacking for 3-D Integration

Bernard Aspar, *Managing Director BU Track, Soitec*

- Smart Stacking™ technology, low temperature molecular bonding of partially or fully processed wafers combined with high-precision wafer thinning
- Low-temperature Smart Cut™ technology, low-temperature oxide-oxide molecular bonding and atomic-level cleaving
- Metal-to-metal direct bonding at wafer level
- Engineered substrates for 3-D

Looking Beyond TSV for 3-D IC Technology

Sang-Yun Lee, *CEO, BeSang*

- Advanced emerging 3-D IC approach
- Simplified wafer alignment
- Unrestricted 3-D interconnects
- Provides high performance with millions of 3-D interconnects

11:45 am – 1:00 pm Lunch

Wafer Handling Leads the Way on Manufacturing

Efficient CAPEX Utilization for Thin Wafer Handling

Wilfried Bair, *General Manager, Wafer Bonder Division,*

SUSS MicroTec

- Multi-process equipment platform
- Switch processes as new materials come to market
- Incremental capacity (ROI)
- Short time to market with close material and equipment supplier alignment
- Process and material overview for TMAP, 3M, Brewer Science, and DuPont HD MicroSystems

Thin Wafer Handling and Chip Stacking for 3-D Integration

Thorsten Matthias, *Director of Technology, EV Group*

- Handling and processing of ultra-thin wafers
- Die-to-wafer integration schemes
- High precision alignment systems with sub-micron accuracy
- Wafer bonding

TOK Thin Wafer Handling System and Resist Technologies for TSV Application

Soji Otaka, *Business Development Section,*

Tokyo Ohka Kogyo Co., Ltd.

- Thin-wafer, low-stress bonding and debonding concept
- Bonder/debonder tool and its performance
- Development of adhesive for high temperature process
- Resist solutions for TSV lithography process layers

2:30 pm – 3:00 pm Break

Industry and Government Funded 3-D Efforts – Key Research Outcomes and Resources

IC-Foundry-Agnostic 3-D Integration Technologies

Dorota Temple, *Associate Director, Center for Materials and*

Electronic Technologies, RTI International

- Review of existing IC-foundry-specific and IC-foundry-agnostic 3-D integration approaches
- Advantages and disadvantages in context of requirements of application markets
- IC-foundry-agnostic 3-D integration technologies at RTI: High density 3-D stacked ICs – 3-D packaging – Silicon interposers
- Technology roadmap and access to technology

3-D Activities at CEA-Leti

Mark Scannell, *Microelectronics Programs Manager, CEA-Leti*

- CEA-Leti view and approach to 3-D
- Tool box
- TSV and non-TSV approach
- Results and outlook

ASOI-based Wafer-scale 3-D Circuit Integration Technology

Craig Keast, *Leader, Advanced Silicon Technology Group,*

MIT Lincoln Laboratory

- Overview of 3-D integration process
- Enabling technologies
- Application areas
- Future recommendations

4:30 pm Closing Comments

3-D Architectures for Semiconductor Integration and Packaging

Register online at <http://techventure.rti.org>

RTI International c/o YCC
3208 Oleander Drive, Suite C
Wilmington, NC 28403

REGISTER BEFORE NOVEMBER 24 to receive the early registration rates. After November 24, the conference registration fee will increase by \$100.

	Corporate	Univ/Gov
Conference	\$1199	\$ 799
Symposium	\$ 499	\$ 499
Conference and Symposium	\$1599	\$1199

Corporate Team Discounts—Send two or more people from the same company and receive a \$200 discount off the second and each additional conference registration.

Conference fees include continental breakfasts, lunches, receptions, handouts, and proceedings CD. Symposium fees include luncheon.

Contact Carol Lander at 910.452.0006 (carol@teamycc.com) to register by phone, to pay by check, or to request an invoice. Confirmation will be sent to each registrant.

On-site registration/payment is an additional \$100. If you are unable to attend, proceedings may be purchased for \$499. Registration is fully refundable until December 2, after which a \$300 service charge will apply. Substitutions may be made at any time at no charge.

Exhibits and Sponsorships

EXHIBITS: Showcase your products or services by reserving table-top exhibit space. The exhibit area will be located near the main conference room.

Exhibit Table (registered to attend)	\$1000
Exhibit Table	\$1500

SPONSORSHIPS: Increase your company and product exposure at this conference and in the industry by sponsoring a luncheon or evening reception. Call Carol Lander at 910.452.0006 (carol@teamycc.com) for details.

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