

3D Architectures for Semiconductor Integration and Packaging

Assessing Technological Developments,
Applications, and Key Enablers

31 OCT – 2 NOV 2006

San Francisco Airport Marriott, Burlingame, California

3D integration and packaging of semiconductor devices is gaining noticeable momentum within the semiconductor community. Once only a research curiosity, various forms of 3D integration and packaging are now reaching commercialization, and many continued advancements are expected in the near future. 3D architectures have clearly emerged as a serious contender in the challenges of meeting performance, cost, and size demands for semiconductor devices and products through this decade and beyond.

Continuing upon the success of the first two conferences held in 2004 and 2005, this year's conference will assess key enabling technologies, the industry dynamics, and applications driving commercialization of this emerging technology today, and it will examine the opportunities and challenges that lie beyond. With presentations and participants from leading companies and organizations in the international community, the conference is aimed at providing information that is critical to planning ongoing and future business and technical efforts in this important new arena. Participants will have the opportunity to learn — from presentations and networking with industry leaders — the status of competing technology solutions, commercialization plans, and the key enablers to near- and long-term applications and market opportunities.

3D Architectures for Semiconductor Integration and Packaging targets senior-level technologists, managers, and business executives from the world's leading companies and research institutions. It addresses a full range of interests for designers, manufacturers, suppliers, and end users.

Presentations from

ALLVIA, Inc.
Amkor Technology, Inc.
BeSang Inc.
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Cubic Wafer, Inc.
Elpida Memory, Inc.
EV Group
FlipChip International, LLC
Freescale Semiconductor, Inc.
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3D SiP or 3D SoC:

Applications and Process-Design Implications

See inside cover for more information . . .

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today for registration information!

Join us at the
Preconference Symposium

3D SiP
OR
3D SoC

Applications and
Process-Design
Implications

31 October 2006 1:00pm–5:00pm

This Preconference Symposium will explore 3D System-in-Package (SiP) versus 3D System-on-Chip (SoC) approaches to integrating and packaging advanced functionality into state-of-the-art semiconductor devices. Insights into advantages and disadvantages of each for leading market applications, as well as the process and design implications of emerging 3D and other approaches to SiP and SoC, will be provided. Topics will cover:

- Wafer-level processing infrastructure to support emerging 3D packaging schemes
- Overview of wafer- and die-level process technologies in development throughout the industry
- Emerging 3D packaging schemes: 3D flip chip, wafer-level die stacking, embedded die packaging
- Leading approaches to 3D interconnects: bonding and vias
- Design and manufacturing issues: implications of process needs on design
- Performance/cost advantages and disadvantages
- Determining which approach is best for different applications

Attend to learn from these leading industry experts.

Ted Tessier, CTO
FlipChip International, LLC

Robert Patti, CTO
Tezzaron Semiconductor

Paul Enquist,
CTO and VP, R&D
Ziptronix, Inc.

John Trezza,
President and CTO
Cubic Wafer, Inc.

Moshe Bunyan,
Director 3D/Advanced CSP Products
STATS ChipPAC

Gain important insights into SiP and SoC in this interactive Preconference Symposium.

Hotel Information

The San Francisco Airport Marriott is minutes from the San Francisco International Airport and 15 miles from downtown. Make your reservations by October 9, 2006, and mention that you are attending the RTI 2006 3D Architectures Conference to receive the \$149 room rate.

San Francisco Airport Marriott
1800 Old Bayshore Highway
Burlingame, CA 94010
800.228.9290
www.marriott.com/sfobg

31 October

1:00pm – 5:00pm
Preconference Symposium

6:00pm – 8:00pm
Registration and Welcome Reception

1 November

6:45am – 7:45am Registration and Breakfast

7:45am Welcome/Opening Comments

Conference Co-Chairs:

Wilfried Bair

VP Business Development, Ziptronix, Inc.

Bart Swinnen

Program Manager, IMEC

KEYNOTE SESSION
Measuring Progress and Opportunity

3D Wafer Level Interconnect: The Next Wave of Electronic Packaging

Neil Moskowitz, Senior Consultant

Prismark Partners LLC

- Electronics interconnect trends
- Driving forces for high-interconnect density
- Wafer-level interconnect vs. alternatives: SiP, SoC, MCM, stacked packages
- Market forecast

Industry Progress Toward 3D and Signposts on the Road Ahead

Phil Nyborg, CEO

Ziptronix, Inc.

- Industry scorecard for 3D commercialization
- Technology segmentation: competing and complementary technologies
- Signposts toward commercial needs

Impact of 3D on Roles of Foundry —
Packaging — Assembly & Test

Challenges in 3D Packaging

Mehdi Hosseini, Senior Analyst

Friedman Billings Ramsey and Company, Inc.

- Testing issues and industry plans
- Roles of foundries and assembly-and-test subcontractors
- Yield considerations for 3D packaging

Silicon Foundry Perspective of 3D Technology

Marco Racanelli, VP Engineering

Jazz Semiconductor

- Intercept of wafer foundry and packaging as it relates to 3D technologies
- How SiP concept enabled by 3D technology can impact the roadmap of the wafer foundry
- Through-wafer via efforts at Jazz Semiconductor

10:00am – 10:30am Break

Emerging 3D Technologies, Market Drivers,
and Applications

3D Package Selection — Key Design, Technical, Business, and Logistic Factors

Lee Smith, Senior Director, New Business Development
Amkor Technology, Inc.

- Multimedia handsets, logic and memory integration, trends and requirements
- Candidate 3D package technologies
- Package on Package (PoP) solution
- Market outlook and applications for PoP
- Industry standards and infrastructure
- Cost and performance

Programmable System-in-Package (PSiP)

Arifur Rahman, Senior Staff

Xilinx, Inc.

- Enabling technologies
- Applications
- The PSiP ecosystem

Cost Savings Potential of 3D Integration for Differentiated Technologies

Scott Pozder, Advanced Interconnect Group

Freescale Semiconductor, Inc.

- System needs drive choice of architectures
- Economics of differentiated technologies
- Package I/O limitation on ultimate 3D packing
- Other system considerations for 3D architectures

Noon – 1:30pm Luncheon

Future Potential of 3D Technologies Using Post-Silicon Process and Devices

Shinobu Fujita, Senior Research Scientist

Toshiba Corporation

- Trend of future 3D from Si to post-Si
- Comparison of interconnect delay between Si-based 3D and post-Si-based 3D
- Comparison of bandwidth between Si-based 3D and post-Si-based 3D
- Network-on-chip based on post-Si 3D technologies

A Contactless 3D Technology

Roberto Canegallo, Program Manager

STMicroelectronics

- Package level integration: overview
- 3D high-speed wireless communication approach
- Assembly process flow and alignment options
- Key applications

The Next Generation Package Technology for Higher Performance and Smaller Systems

Kangwook (Kris) Lee, Senior Engineer, Memory Division

Samsung Electronics Co. Ltd.

- Samsung's 3D chip stacking technology, WSP
- Market applications and requirements
- Challenges for the business

Stacked Memory Chip Technology Development

Hiroaki Ikeda, Principal Professional

Elpida Memory, Inc.

- Elpida Memory, NEC Electronics, and Oki Electric Partnership
- TSV process
- Design for DRAM

Assessing Process and Equipment
Infrastructure — Session 1

Manufacturing Solutions for Wafer-to-Wafer and Chip-to-Wafer 3D Integration Schemes

Thorsten Matthias, Product Manager
EV Group, E. Thalner GmbH

- Wafer alignment and bonding — recent advances
- Via-first vs. via-last process flow
- Face-to-face vs. back-to-face integration
- In situ wafer pretreatment (cleaning, plasma activation, coating)
- Multiple layer processes
- Equipment roadmaps

Die and Wafer Level 3D Packaging for Advanced ICs and Microelectronics

Henry Chou, Product Manager, Flip Chip Division
Laurier Incorporated

- Market drivers and cooperative efforts
- Applications — memory, imaging sensors, other
- Bonding methods — die-to-wafer/wafer-to-wafer pros and cons, 3D stacking, MEMS
- Assembly costs and quality data
- Future trends

6:30pm — 8:30pm Evening Reception

2 November

6:45am — 7:45am Continental Breakfast

On the Front Line of Commercialization

3D Scaling to Production

Robert Patti, CTO

Tezzaron Semiconductor

- Standard products: Why and when?
- 3D ASICs: A mixed approach
- Qualification: What's important?

3D Chip Stacking — Through-Die Via Development

John Trezza, President and CTO

Cubic Wafer, Inc.

- Process
- Yield
- Reliability
- Performance

Single Chip 3D Memory

Sang-Yun Lee, President and CEO

BeSang Inc.

- Technology overview
- Market demands on single-chip 3D memory
- Comparison with other 3D package approaches

3D-LSI and Its Key Supporting Technologies

Makoto Motoyoshi, VP and Managing Director

ZyCube Co., Ltd.

- Cavity-type CSP image sensor fabricated by 3D technology
- Fine pitch micro-bumping technology
- Fine pitch vertical interconnection technology



Headline Sponsor

EVG manufactures leading-edge wafer bonders, mask and bond aligners, photoresist coaters, and cleaners for MEMS, nanoimprint, and semiconductor market segments. As the technology and market leader for wafer bonding systems, EVG has set worldwide industry standards in aligned wafer bonding and double-side lithography. EVG's systems are installed worldwide in high-volume production environments as well as research and development facilities.

Direct Bond Interconnect

Paul Enquist, Vice President R&D and CTO

Ziptronix, Inc.

- Technology overview
- Scalability and manufacturability
- Post-bond processing
- Reliability

10:15am — 10:45am Break

Developments in Design Tools for 3D

Design Space Exploration for 3D IC Design

Yuan Xie, Assistant Professor

The Pennsylvania State University

- EDA design tools to enable 3D IC design exploration
- Thermal aware design
- Microarchitecture components design

CAD Tools for 3D System Design

Lisa McIlrath, President/CEO

R³Logic, Inc.

- Layout
- Floor planning
- Thermal/electromagnetic effects
- Demonstration

Design for 3D

Paul Franzon, Alumni Distinguished Professor of Electrical
and Computer Engineering

North Carolina State University

- 3D design issues and benefits
- Case studies

12:15pm — 1:30pm Luncheon

Emerging Applications and Capabilities of
3D Architectures

3D Architecture for Power Delivery to Microprocessors and ASICs

James Jian-Qiang Lu, Professor

Rensselaer Polytechnic Institute

- Power delivery bottlenecks
- Use and benefits of 3D architecture for power delivery
- DC-DC converter prototype design
- Future opportunity and plans for power delivery using 3D hyper-integration of converters, passives, and systems

3D Integration: A Technology for System-of- Systems-on-a-Chip (S2OC)

Ken Williams, Director, Center for Materials and Electronic
Technologies

RTI International

- Paradigm shifting application — avionics for UAVs

- New approach for 3D integration of microsystems combining vertical interconnects, MEMS, advanced flip chip technology, and embedded passives
- 3D integration approach for high-density interconnects
- Through-wafer vias for thermal management
- 3D embedded passives

3D Integration by Direct IC Stacking: 3D-SIC (Stacked IC)

Bart Swinnen, Program Manager, Wafer Level Packaging
3D-SiC

IMEC

- Positioning different approaches to 3D integration
- Exploring the limits of the through-Si via process for 3D-SiC
- Wafer thinning on carrier
- Limitations of direct stacking and bonding

3:00pm — 3:15pm Break

Innovations in 3-D Circuit Integration via Direct Bonding Technologies

Nelly Kernevez, Transfer of Films and Circuits Laboratory
Leader

CEA-DRT/LETI

- Materials and process developments drive 3D integration approaches
- Direct bonding and Smart Cut™ layer transfer for Si, SOI, GeOI, SSOI and other substrate types — a crucial role in circuit transfer and new 3D integration schemes
- Device examples and performance achievements for advanced front- and back-end architectures
- Enabling multiple IC functions and smart integrated hetero-structures and systems

Assessing Process and Equipment
Infrastructure — Session 2

Vertical Integration: A Confederacy of Alignment, Bonding, and Materials Technologies

Sharon Farrens, Chief Scientist, Wafer Bonder Division

SUSS MicroTec

- Alignment strategies for 3D integration and relationship to bonding methods
- Pros and cons of wafer bond/debond techniques
- Bond alternatives without handle wafers
- Error analysis in alignment of 3D structures
- Special handling concerns

Commercialization of Thru-Silicon Via Foundry Capabilities

Sergey Savastiouk, CEO

ALLVIA, Inc.

- Commercialization report
- Foundry capabilities
- Thru-silicon via applications

4:45pm Closing Comments

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Register online at

<http://techventure.rti.org>

REGISTER BEFORE OCTOBER 10 to receive the following early registration rates. After October 10, the conference registration fee will increase by \$100.

	Corporate	Univ/Gov
Conference	\$1199	\$ 799
Symposium	\$ 499	\$ 499
Combined Conference & Symposium	\$1599	\$1199

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Conference fees include continental breakfasts, luncheons, receptions, handouts, and proceedings CD. Symposium fees include refreshments, handouts, and symposium proceedings CD.

Or contact Kim Dicso at 910.452.0006 (kim@teamycc.com) to register by phone, to pay by check, or to request an invoice.

If you are unable to attend, proceedings may be purchased for \$499. Registration is fully refundable until October 23, after which a \$300 service charge will apply. Substitutions may be made at any time at no charge.

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Exhibit Table (registered to attend) \$ 699

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